


EPV Technologies	Newsletter
	<p><b>In this number</b></p> <p><b>1) Tech Papers – HiperDispatch Logical Processors and Weight Management - Part 2</b></p> <p><b>2) Tech News – Upcoming events</b></p> <p>CMGAE &amp; EuroCMG 2008, Wien, 9-10 October  UKCMG Free Forum, London, 14 October  EPV User Group 2008, Rome, 21 October  GSE UK, Kenilworth, 28-29 October</p> <p><b>3) Tech Notes - EPV for z/OS V8 planned enhancements</b></p>
<p>29 August 2008 - Number 8</p>	<p>Past numbers of this newsletter are available on the web at <a href="http://www.epvtech.com">http://www.epvtech.com</a></p>
<p>This message contains news related to EPV products produced and distributed by EPV Technologies. The EPV products suite answer problems such as <b>Managing Performance, Tuning and Capacity Planning</b> on the most common platforms, <b>allowing huge savings on HW and SW costs</b>. Greater details and information on EPV products and solutions can be found at <a href="http://www.epvtech.com">http://www.epvtech.com</a> or writing to <a href="mailto:epv.info@epvtech.com">epv.info@epvtech.com</a>.</p>	
<p><i>All the mentioned trademarks belong to their respective companies.</i></p>	
<p><b>1) Tech Papers</b></p>	<p><b>HiperDispatch Logical Processors and Weight Management - Part 2</b></p>
<p><b>Abstract</b></p>	<p>Fabio Massimo Ottaviani - EPV Technologies</p>
<p>In the last few years, the power and number of the physical processors available on mainframe hardware has greatly increased, allowing the concentration of a much higher number of LPARs than before on a single machine.</p> <p>A side effect of this high number of LPARs is an increase of the number of defined logical processors compared to the number of physical CPs.</p> <p>These factors tend to reduce the probability for a logical processor to be re-dispatched to the same physical processor and therefore reuse instructions and data previously loaded in the Level 1 cache (the amount of cache memory dedicated to each processor).</p> <p>A L1 cache miss will cause data and instructions to be loaded from the Level 2 cache (the cache memory shared among all the physical processors packaged in a book). Performance degradation and overhead occurs when this happens because the access to L2 cache will require more CPU cycles to be performed. However if the logical processor has been dispatched to a different physical processor which belongs to a different book, the required instructions and data have to be loaded from the previously used L2 cache and performance degradation and overhead can be much worse.</p> <p>HiperDispatch has been designed to minimise the number of L1 cache misses and, if a L1 cache miss occurs, to maximise the probability of finding instructions and data in the L2 cache of the book where the logical processor is dispatched.</p> <p>To reach this goal, a new weight called polarization weight has been introduced; polarization weight is a key element in the HiperDispatch design because it is the way z/OS uses to give PR/SM indications on how logical processors should be dispatched to the physical processors. This paper, using real life examples, will discuss:</p> <p>PR/SM and IRD logical processors and weight management (Part 1);  HiperDispatch logical processors and weight management (Part 2).</p> <p><i>If you want to receive the paper you can reply to this e-mail writing "HiperDispatch Logical</i></p>	

**CMGAE & EuroCMG 2008, Wien, 9-10 October**

CMGAE 2008 will be held in Wien on October 9-10. The conference will host the 11th edition of EuroCMG.

EPV Technologies will present the paper: "Bigger Savings Using New z Technologies".

More details at: <http://www.cmg-ae.at/>

**UKCMG Free Forum, London, 14 October**

The new UKCMG Free Forum will take place on the 14th October 2008 at the CBI Conference Centre, Centrepont, London, WC1 1DU.

This one-day conference will keep you abreast of developments and in touch with key IT people. There will be a multi-tracked agenda and a full table top exhibition running alongside the conference allowing you the opportunity to network with other key IT people.

Inspired Solutions, official distributor of EPV products in UK and Ireland, and EPV Technologies will sponsor the conference.

EPV Technologies will also present the papers:

- "Estimating GCP, zAAP and zIIP Latent Demand"
- "Managing Websphere-DB2 transactions with WLM"

More details at: <http://www.ukcmg.org.uk/ifOct2008.html>

**EPV User Group 2008, Rome, 21 October**

The 6th EPV User Group will be held in Rome, at the Residenza di Ripetta, on October 21st 2008.

The EPV User Group is a "not to miss" event for all Performance Analysts; it will give you the opportunity to share ideas with qualified experts and to listen to some of the EPV customers experiences.

Preliminary Agenda

09:30 Registration

10:00 Welcome and introduction, EPV Technologies

10:15 EPV for z/OS user experience, Sieghart Seith, FIDUCIA (to be confirmed)

10:45 What's new in EPV for z/OS 8.0, EPV Technologies

11:15 Coffee break

11:45 EPV for Unix and Windows user experience, Paolo Di Martino, POSTE ITALIANE (to be confirmed)

12:15 EPV Parser for SMF user experience, Giorgio Grigolo, T-SYSTEMS (to be confirmed)

12:45 What's new in EPV for DB2 3.0, EPV Technologies

13:15 Lunch

14:30 10 Ways to Save Money on the Mainframe, EPV Technologies

16:00 User Group end

Mark the day in your agenda to avoid missing this event.

### **GSE UK, Kenilworth, 28-29 October**

The GSE UK Conference 2008 will be held in Kenilworth on 28th-29th October.

GSE is the UK's premiere independent annual event addressing the challenges of delivering & maintaining solutions based on IBM architecture & open standards.

EPV Technologies will present the papers:

- "Estimating GCP, zAAP and zIIP Latent Demand"
- "Managing Websphere-DB2 transactions with WLM"
- "Bigger Savings Using New z Technologies"
- "Software Consolidation on the Mainframe"

More details at: <http://www.gse.org.uk/>

### **3) Tech Notes**

#### **EPV for z/OS V8 planned enhancements**

EPV for z/OS V8 will include three new visions:

- Throughput Vision
- User Vision
- User Trend Vision

Throughput Vision has been isolated from the current Workload Vision to improve customers navigation and usability.

User and User Trend are brand new visions; they will allow customers to request reports to control specific CICS, IMS transactions, batch jobs and A.S. throughput, performance and resource usage.

The following major enhancements have been already developed or are in the final development stages:

#### **a) USABILITY**

- New GUI based on "button" menus
- New design to set machine target capacity (CPU, AAP and IIP) allowing to use MIPS tables or EPV automatic algorithm
- Automatic check to avoid to use obsolete MIPS values when customers fix them in EPV provided user exits
- Shift created in the HTML phase not fixed at load time
- Bookmark function extended to all trends reports
- Sortable columns in trend reports where possible
- Day of the week added in all daily trend reports
- Customizable thresholds by user exits
- GMT/User time support

#### **b) TECHNICAL CONTENT**

- Hiper Dispatch support
- Blocked Workloads support
- Ficon Directors configuration and activity
- VSM configuration and activity
- CF CPU usage by structure
- XCF activity including both CTC and CF structures
- New WLM Work Manager states support
- Estimate of possible WLC savings using more AAP/IIP
- Estimate of possible WLC savings delaying low importance WLM workloads

EPV for z/OS V8 will be released based on the following plan:

- October 2008, Beta Version
- November 2008, Managed Availability
- December 2008, General Availability

If you've received this mail by mistake, or you don't want to receive any more such messages, please send a mail to [epv.info@epvtech.com](mailto:epv.info@epvtech.com) with a subject "**REMOVE**". You'll be promptly removed from the list.

If you want to subscribe to this list you can do that simply sending a mail to [epv.info@epvtech.com](mailto:epv.info@epvtech.com) with a subject "**SUBSCRIBE**".